Claim Listing:

Please replace all previous claim listings with the following claim listing.

1-11. (Cancelled)

12. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a gate line including a gate insulation pattern, a gate electrode that comprises a doped polysilicon layer and a metal silicide layer which are sequentially stacked on the semiconductor substrate;

a spacer formed on a sidewall of the gate line;

a conductive line pattern disposed on the gate line; and

an interlayer dielectric on the semiconductor substrate having a top surface that is coplanar with a top surface of the gate line;

wherein the conductive line pattern is parallel to the gate line and electrically connected to the gate electrode.

13-17. (Cancelled)

18. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern has at least the same length as the gate line.

19. (Original) The semiconductor device of Claim 12, wherein the conductive line pattern is made of metal.

20. (Previously Presented) The semiconductor device of Claim 14, wherein the conductive line pattern bridges at least one gap in the metal silicide layer.

21. (Previously Presented) The semiconductor device of Claim 12, wherein the conductive line pattern decreases the resistance of the gate electrode.

22. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a first gate line and a second gate line on the semiconductor substrate, the first and second gates lines being collinear and spaced apart from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern; and

a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other.

23. (Original) The semiconductor device of Claim 22, wherein the first and second gate lines comprise a doped polysilicon layer.

24. (Previously Presented) A semiconductor device comprising:

a semiconductor substrate;

a first gate line and a second gate line on the semiconductor substrate and spaced apart from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern;

a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other;

wherein the first and second gate lines each comprise a metal silicide layer on a doped polysilicon layer.

25. (Withdrawn) A semiconductor device comprising:

a semiconductor substrate;

a first gate line and a second gate line on the semiconductor substrate and spaced apart

from each other, the first gate line including a first gate electrode stacked on a first gate insulation pattern, and the second gate line including a second gate electrode stacked on a second gate insulation pattern;

a conductive line pattern on the first and second gate lines, wherein the conductive line pattern has a first portion parallel to the first gate line and a second portion parallel to the second gate line, and wherein the conductive line pattern electrically connects the first and second gate electrodes with each other;

a spacer disposed on a sidewall of the first and second gate lines; and

an interlayer dielectric covering the semiconductor substrate that includes a groove that exposes top surfaces of the first and second gate line;

wherein the conductive line pattern is disposed in the groove in the interlayer dielectric.

26. (Withdrawn) The semiconductor device of Claim 25, further comprising an etch-stop layer between the semiconductor substrate and the interlayer dielectric, wherein the etch-stop layer has an etch selectivity with respect to the interlayer dielectric.

27. (Previously Presented) The semiconductor device of Claim 24, further comprising an interlayer dielectric on the semiconductor substrate that is planarized to the height of the first and second gate lines, wherein the conductive line pattern is also disposed on the interlayer dielectric between the first and second gate lines.

28. (Original) The semiconductor device of Claim 22, wherein the first portion of the conductive line pattern is at least the same length as the first gate line, and the second portion of the conductive line pattern is at least the same length as the second gate line.

29. (Original) The semiconductor device of Claim 22, wherein the conductive line pattern is made of metal.

30. (Previously Presented) The semiconductor device of Claim 24, wherein the

conductive line pattern bridges at least one gap in the metal silicide layer.

31. (Previously Presented) The semiconductor device of Claim 22, wherein the conductive line pattern decreases the resistance of the gate electrode.

32-49. (Canceled).

50. (Previously Presented) A semiconductor device, comprising:

a gate electrode on a semiconductor substrate, the gate electrode including a polysilicon layer and a metal silicide layer which are sequentially stacked; and

a conductive line pattern on the gate electrode, the conductive line pattern extending in a first direction and being in contact with the gate electrode along the first direction,

wherein the first direction is substantially parallel to a longitudinal direction of the gate electrode.

51. (Previously Presented) The semiconductor device of Claim 50, further comprising a gate insulation pattern between the semiconductor substrate and the gate electrode.

52. (Previously Presented) The semiconductor device of Claim 50, wherein the conductive line pattern is formed of at least one of aluminum, tungsten, titanium, tantalum, or copper.

53. (Withdrawn) The semiconductor device of Claim 50, further comprising an interlayer dielectric on the semiconductor substrate, and wherein the conductive line pattern is disposed in a groove in the interlayer dielectric, and the conductive line pattern has a top surface that is coplanar with a top surface of the interlayer dielectric.

54. (Withdrawn) The semiconductor device of Claim 53, further comprising a plug line penetrating the interlayer dielectric layer, the plug line being electrically connected to the semiconductor substrate outside of the gate electrode and extending in the first direction.

55. (Previously Presented) The semiconductor device of Claim 50, further

comprising a planarized interlayer dielectric on the semiconductor substrate,

wherein the top surface of the planarized interlayer dielectric and the top surface of the gate electrode are substantially the same height above the semiconductor substrate.

56. (Previously Presented) The semiconductor device of Claim 50, further comprising a second gate electrode with the same material as the gate electrode, wherein the conductive line pattern is in contact with the second gate electrode.

57. (Previously Presented) The semiconductor device of Claim 56, wherein the second gate electrode extends in the first direction.

58. (Previously Presented) The semiconductor device of Claim 56, wherein the second gate electrode extends in a second direction, and wherein the conductive line pattern further extends along the second direction.

59. (Withdrawn) The semiconductor device of Claim 54, further comprising a second gate electrode on the semiconductor substrate, wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and wherein the conductive line pattern electrically connects the gate electrode and the second gate electrode.

60. (Previously Presented) The semiconductor device of Claim 55, further comprising a second gate electrode on the semiconductor substrate, wherein the second gate electrode comprises a metal silicide layer on a polysilicon layer, and wherein the conductive line pattern electrically connects the gate electrode and the second gate electrode.

61. (Withdrawn) The semiconductor device of Claim 56, further comprising an interlayer dielectric on the semiconductor substrate, and wherein the conductive line pattern is disposed in a groove in the interlayer dielectric.

62. (Withdrawn) The semiconductor device of Claim 61, wherein the interlayer dielectric includes a second groove, and wherein the device further comprises a plug line that

electrically connects a source/drain region in the semiconductor device with a source/drain region of an adjacent semiconductor device.

63. (Previously Presented) The semiconductor device of Claim 50, wherein the conductive line pattern is formed of a different material than the metal silicide layer.

64. (Previously Presented) The semiconductor device of Claim 12, wherein the conductive line pattern is formed of a different material than the metal silicide layer.

65. (Previously Presented) The semiconductor device of Claim 24, wherein the conductive line pattern is a metal line pattern that is on the metal silicide layer.

66. (Previously Presented) The semiconductor device of Claim 65, wherein the conductive line pattern bridges at least one gap in the metal silicide layer.

67. (Withdrawn) The semiconductor device of Claim 24, further comprising a spacer disposed on a sidewall of the first and second gate lines; and

an interlayer dielectric covering the semiconductor substrate that includes a groove that exposes top surfaces of the first and second gate line;

wherein the conductive line pattern is disposed in the groove in the interlayer dielectric.

68. (Withdrawn) The semiconductor device of Claim 25, wherein the first and second gate lines each comprise a metal silicide layer on a doped polysilicon layer.

69. (Withdrawn) The semiconductor device of Claim 25, wherein the conductive line pattern is a metal line pattern that is on the metal silicide layer.